IN THE CLAIMS

Please amend Claim 5 as follows:

1. (Original) A unit cell for a digital to analog conversion circuit comprising;
- a current source (CS);
- a first data switch (S1) coupled to the current source (CS);
- a second data switch (S2) coupled to the current source (CS);
- a first phase switch (Phi1) coupled between the current source (CS) and the first data switch (S1);
- a second phase switch (Phi2) coupled between the current source (CS) and the second data switch (S2);
- a controller arranged to switch between the first (Phi1) and second (Phi2) phase switches in a Break Before Make alternating sequence, and to switch the first (S1) and second (S2) data switches in a Make Before Break sequence.

2. (Original) A unit cell for a digital analog conversion circuit according to claim 1 wherein the phase switches (Phi1 and Phi2) are formed of MOS transistors.

3. (Previously Presented) A unit cell for a digital analog conversion circuit according to claim 1 wherein the data switches (S1 and S2) are formed of MOS transistors.

4. (Previously Presented) A unit cell according to claim 1 wherein the data switches (S1 and S2) each comprise first (D1+, D2+) and second (D1-, D2-) transistors with common connected sources/emitters, with the drains collectors coupled respectively to first (Outputs)and second (Out min) output lines.

5. (Currently Amended) A unit cell according to claim 4 wherein a third transistor (D1d, D2d) is ~~preferably~~ provided for each data switch (S1, S2) wherein the source/emitter of each of the third transistors (D1d, D2d) is coupled in common with the respective first (D1+, D2+) and second (D1-, D2-) transistors and with its drain/collector coupled to a third output line (Outdump).

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6. (Previously Presented) A unit cell according to Claim 4 wherein the gate/bases of each transistor are coupled to the digital data input.

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